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ABSTRACT

A DSP device is disclosed having multiple DMA controllers with global DMA access to all volatile memory resources in the DSP device. In a preferred embodiment, each of the DMA controllers is coupled to each of the memory buses and is configured to control each of the memory buses. A memory bus multiplexer may be coupled between the subsystem memory bus and each of the DMA controllers, and an arbiter may be used to set the memory bus multiplexer so as to allow any one of the DMA controllers to control the memory bus. The memory bus may also be controlled by the host port interface via the memory bus multiplexer. A round-robin arbitration technique is used to provide each of the controllers and the host port interface fair access to the memory bus. This approach may advantageously provide increased flexibility in the use of DMA controllers to transfer data from place to place, with only a minimal increase in complexity.